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(71) Applicant: Toshiba Corp, Toshiba Tsushin Syst Eng KK
(72) Inventor: Watanabe Hiroyuki, Katayama Taizo, Tsuchiya Shigeru
(54) Title of the invention: Communication system
(57) Abstract:
Problem to be solved: To allow a device itself to apply changeover control to a proper clock extract destination automatically based on clock extract destination information registered in advance in the case that a clock error is detected when a clock is extracted from an external clock source.
Solution: In the midst of clock extraction by a line number A with priority 1 registered in a clock extract line priority table, when a problem management section 6 detects a clock error, the section 6 gives an instruction of a changeover request of the clock extract destination to a clock control section 7. Then the clock control section 7 receiving an instruction of the clock extract destination changeover request applies changeover control to a clock

destination from the line number A registered to priority 1 to a line number B with 2nd priority.

[Claims]
[Claim 1] A communication system which supplies a clock which extracted and this extracted a clock from a source of an external clock through a circuit to each node device of a system, and communicates synchronizing with this clock, including a memory means which stores priority information which shows in advance of clock extraction corresponding to circuit information connected to the mentioned above source of an external clock, a clock extraction point switching control means which performs switching control of the clock extraction point based on information stored by the mentioned above memory means when a clock abnormality is detected.
[Claim 2] The communication system according to claim 1 performing switching control of the clock extraction point again based on information stored by the mentioned above memory means when it includes a means to judge the normality of this clock and a clock abnormality is detected as a result of the mentioned above judgment before using this clock within a system, after the mentioned above clock extraction point switching control means carries out a clock extraction point change.
[Claim 3] The communication system according to claim 1 characterized by that mentioned above each node device takes composition connected to ring shape according to a transmission line where transmission directions differ.
[Claim 4] A communication system which communicates synchronizing with a clock which has a selection circuitry

which carries out the selected output of any one network clock extracted from a signal received from a public network from an external clock extracted from a signal received from a source of an external clock oscillation, and a running clock oscillated from an oscillator mounted in a self-device, and carried out the selected output by the mentioned above selection circuitry characterized by including a clock detection means to perform detection of a clock stop, and detection of abnormalities in a clock rate for every clock in the preceding paragraph of the mentioned above selection circuitry, a clock switching control means which controls a change of a clock which carries out a selected output in the mentioned above selection circuitry according to a result of the mentioned above detection.

[Claim 5] The communication system according to claim 4 characterized by that the mentioned above clock detection means has a clock stop judging means which detects a clock which exceeds a given period for the mentioned above every clock, and is judged to be a clock stop.

[Claim 6] The communication system according to claim 4 or 5 characterized by that the mentioned above clock detection means has a clock rate abnormality determining means that detects a clock below a given period for the mentioned above every clock, and judges that it is an unusual clock rate.

[Claim 7] A communication system which supplies a clock extracted from a source of an external clock to each node device of a system, and communicates synchronizing with this clock, including a clock extracting

means which extracts a clock from the mentioned above source of an external clock, a data forwarding means to receive a normal clock outputted from the mentioned above clock extracting means, and to perform sending operation of valid data or invalid data, a clock normality verifying means which checks the normality of a clock which judges whether data was sent out from the mentioned above data forwarding means at the time of a power supply standup, and is outputted from the mentioned above clock extracting means.
[Claim 8] The communication system according to claim 7 characterized by that the mentioned above node device communicates by an Asynchronous Transfer Mode (ATM).

[Detailed description of the invention]
[0001]
[Field of the invention] This invention relates to the communication system which chooses any one of the clock of a public network, the clock of an external office or running clocks as a master clock, and communicates synchronizing with the this chosen master clock.
[0002]
[Description of the prior art] Conventionally, in the clock abnormality detection solution in this kind of communication system, when a clock abnormality was detected on a ring network, performing loopback for the node device connected with the transmission line which abnormalities generated automatically was performing clock relief at the time of clock abnormality detection, for example.

[0003] However, in this conventional communication system, when the clock source was being extracted from external devices (SDH and the like), as clock extraction solution at the time of detecting a clock abnormality, the clock extraction point needed to be manually changed by the maintenance person with the network management device which supervises each node device.
[0004] In the conventional communication system, as shown on drawing 9, the node device 100 (next a «switchboard») carries the clock board 1100 in a system. The operation of this clock board 1100 was generated and distributed by carrying out dividing to the 8 kHz clock of a basis in the form where a synchronization is taken in the PLL circuit which has in an inside a clock which each substrate needs to the substrate which has each function in the switchboard 100, the clock of 8kHz that consisted of the following 3 kinds is a master clock. 3 kinds of 8 kHz clocks used as the mentioned above master clock, 1st is connecting with other nets and terminal and the like by cell base, a frame relay, and the like, the interface board 1200 which communicate, the 8 kHz clock compounded with the signal received from the public network 200 (network clock) was extracted, the 2nd receives clocks, such as 64k+8k which an external office serves as the source 300 of dispatch, and is sent out, and by which AMI coding was carried out, the 8-kHz clock which and is compounded (external clock) was extracted, the 3rd is the 8 kHz clock (running clock) sent from the crystal oscillator 1101 carried in a self-board.
[0005] Here, the composition of the clock board 1100 mounted in the conventional switchboard 100 is shown on

drawing 10. In drawing 10, 3 mentioned above 8 kHz clocks are chosen through the selector (IC) 1102 within the clock board 1100, and the selected clock, dividing generation is carried out in what is then distributed to each of other substrate in the switchboard 100 as an 8 kHz clock, and PLL circuit 1103 and the frequency divider 1104 at various frequency, and it is distributed to each of other same substrate in the switchboard 100. In PLL circuit 1103, when it is judged that the PLL cycle was removed above the fixed cycle, it is judged as a step out and information is raised as an alarm. When the 8 kHz clock selected similarly is put in by the clock stop primary detecting element 1105 by the next step and the standup of a clock is not detected by one side as for more than arbitrary cycles, it is the mechanism of having judged it as a clock stop and raising information as an alarm, and after that, the control section 1400 which manages the control facility in the switchboard 100 read such alarm information, and was performing arbitrary processings. For example, when the network clock is chosen by the selector 1102 and a clock stop occurs, the control section 1400 is performing processing which chooses 8 kHz of running by oneself clock by the selector 1102 after malfunction detection.

[0006]

[Problems to be solved by the invention] If it is in the conventional communication system, when the clock is being extracted from the source of an external clock, in the case where a clock abnormality is detected. As the clock extraction point was only manually changed to changing the clock extraction point by a maintenance

person in a network monitor, the time and effort according to a maintenance person became large, and there was inconvenience that hand control could not perform clock relief at an early stage depending on it.

[0007] If it is in the conventional communication system, 1 is chosen from 8 kHz which becomes a network clock, an external clock, and 3 master clocks of a running clock with a clock board, as alarm detection of a PLL step-out, a clock stop, and the like was performed and it was processing by a control section reading information after that, while distributing the frequency clock of after that versatility, when it was effective when the clock of the late cycle exceeding the situation or the arbitrary cycles as which an 8 kHz clock is not inputted was inputted, but the clock of frequency quicker than 8 kHz is inputted, it is possible to have an adverse effect also on the clock which detection of a clock abnormality cannot be performed, but is distributed to each substrate in a switchboard. (For example, in a PLL malfunction detection section, as it will be made to synchronize with the clock and the circuit will operate as like if a reference clock is inputted with a clock quicker than 8 kHz, it will always be in the out of phase abnormal condition of PLL), it becomes impossible to protect the accuracy of the clock generated by dividing. As malfunction detection of the 8 kHz clock used as a master clock is performed by the selector IC again, after changing and changing in the state where there is no informing whether the 8 kHz clock chosen as the next for a change is normal after the clock chosen is judged to be unusual, it is also considered that a clock stop is detected,

and there is a possibility of spoiling communicative reliability in that case.

[0008] Next, when solving the mentioned above problem, extracting the clock from the source of an external clock with this invention and a clock abnormality is detected, while abolishing the time and effort which a maintenance person takes by performing switching control to the clock extraction point automatic and suitable based on the clock extraction point information registered preliminary, it enables the device itself to perform clock relief at an early stage.

[0009] By judging the normality of each clock, before solving the mentioned above problem, and being able to detect a clock quicker than the 8 kHz clock used as a master clock in this invention and choosing by a selector, it enables it to extract a clock at the time of detection of a clock abnormality, as a clock is normal. It enables it to check the normality of a clock in this invention at the time of a device power standup.

[0010]

[Means for solving the problem] In order that this invention may attain the mentioned above purpose, the invention of claim 1 supplies a clock which extracted and this extracted clock from a source of an external clock through a circuit to each node device of a system, and is characterized by that a communication system which communicates synchronizing with this clock includes a memory means which stores priority information which shows in advance of clock extraction corresponding to circuit information connected to the mentioned above source of an external clock, a clock extraction point

switching control means which performs switching control of the clock extraction point based on information stored by the mentioned above memory means when a clock abnormality is detected.

[0011] In the invention of claim 1, in the invention of claim 2, the mentioned above clock extraction point switching control means includes a means to judge the normality of this clock and a clock abnormality is detected as a result of the mentioned above judgment before using this clock within a system after carrying out a clock extraction point change, switching control of the clock extraction point is again performed based on information stored by the mentioned above memory means.

[0012] In the invention of claim 1, the invention of claim 3 takes composition in which the mentioned above each node device connects to ring shape according to a transmission line where transmission directions differ.

[0013] In this invention, in the invention of claim 4, a communication system which communicates synchronizing with a clock which has a selection circuitry which carries out the selected output of any one network clock extracted from a signal received from a public network from an external clock extracted from a signal received from a source of an external clock oscillation, and a running clock oscillated from an oscillator mounted in a self-device, and carried out the selected output by the mentioned above selection circuitry characterized by including a clock detection means to perform detection of a clock stop, and detection of abnormalities in a clock rate for every clock in the preceding paragraph of the mentioned above selection circuitry, a clock switching

control means which controls a change of a clock which carries out a selected output in the mentioned above selection circuitry according to a result of the mentioned above detection.

[0014] In the invention of claim 5, the invention of claim 4 has a clock stop judging means in which the mentioned above clock detection means detects a clock which exceeds a given period for the mentioned above every clock, and is judged to be a clock stop. In the invention of claim 6, the invention of claim 4 or 5 has a clock rate abnormality determining means, the mentioned above clock detection means detects a clock below a given period for the mentioned above every clock, and judge that it is an unusual clock rate.

[0015] In the invention of claim 7, a communication system which supplies a clock extracted from a source of an external clock to each node device of a system, and communicates synchronizing with this clock, including a clock extracting means which extracts a clock from the mentioned above source of an external clock, and a data forwarding means to receive a normal clock outputted from the mentioned above clock extracting means, and to perform sending operation of valid data or invalid data, at the time of a power supply standup, a clock normality verifying means which checks the normality of a clock which judges whether data was sent out from the mentioned above data forwarding means, and is outputted from the mentioned above clock extracting means.

[0016] In the invention of claim 8, in the invention of claim 7, the mentioned above node device communicates by an Asynchronous Transfer Mode (ATM).

[0017]
[Embodiment of the invention] Next, the 1 embodiment according to this invention is described in details with reference to an accompanying drawing.
[0018] First, the 1st invention is explained.
[0019] Drawing 1 is a drawing showing the example of 1 composition of the communication system according to the 1st embodiment of the invention. As shown on drawing 1, with this communication system, a plurality of node devices (A-D) 1 are connected to ring shape with the transmission lines 2a ,2b from which a transmission direction differs, and the composition of the ring network possessing the node monitoring instrument 3 which supervises these each node device (A-D) 1 is shown.
[0020] And in this communication system, a clock is extracted from the source 4 of an external clock, and it communicates synchronizing with this extracted clock.
[0021] As an extraction method of this clock, as shown on drawing 1, it is setting the node device (A) 1 as the external clock synchronous mode (operating state which is got blocked and extracts a clock from the exterior), and a node device (A) will extract a clock from the source 4 of an external clock, for example. And the clock extracted by doing in this way, from a node device (A), using the duplex transmission line 2a, the direction of a node device (B) -> node device (C) -> node device (D) -> node device (A), a clock is supplied to other node devices using duplex transmission line 2b by the direction of a node device (D) -> node device (C) -> node device (B) -> node device (A), and the whole ring network is provided with the clock.

[0022] And in this communication system, when the abnormalities (step-out) of the clock currently extracted from the exterior occur, it is made to relieve the clock extraction at the time of a clock abnormality by registering a node number and a line number into the clock extraction circuit priority table 5 shown on drawing 2. In this invention, this clock extraction circuit table 5, even if each node device (A-D) 1 holds as the clock extraction circuit table 5 which stores the line number of the circuit connected to a self-device, respectively or the node monitoring instrument 3 of the node device (A-D) 1 under surveillance, all information may be held as the clock extraction circuit table 5. In this case, what is necessary is just to have a means which changes the clock extraction point with reference to this table, when a clock problem is detected although explained in details below. Drawing 1 shows the node monitoring instrument 3 and explains the case where the information on all the node devices under surveillance is held.

[0023] And as shown on drawing 2, in this clock extraction circuit priority table 5, while the «node number» information which shows the number of each node device, and these each «node number», «line number» information are registered, which shows the number of the circuit by which matches with information and connection accommodation is carried out for every node device. The «priority» information which shows the priority of clock extraction is given to these each «node number / line number» information, and it stores. And a node device with which «the node number / line number A» set as «the priority 1» are extracting the present clock,

the number of the circuit by which connection accommodation is carried out is shown on the node device, and the table information from «the priority 2» to «the priority n», when a clock abnormality is detected at the clock extraction point of the above «priority 1», it is a clock extraction point information group used in order to change the clock extraction point and to relieve clock extraction. For example, when a clock abnormality occurs at the clock extraction point of the above «priority 1», it changes to the clock extraction point of «the priority 2», and clock extraction is relieved.

[0024] Thus, when the abnormalities (step-out) of the clock currently extracted from the source of an external clock occur in this example, the clock extraction at the time of clock abnormality generating is relievable by registering the line number of the circuit by which connection accommodation is carried out into the number and node device of the node device which becomes the clock extraction circuit priority table 5 preliminary shown on drawing 2 for a clock extraction change.

[0025] The line number registered into the mentioned above clock extraction circuit priority table 5 is a line number of the circuit by which connection accommodation is carried out at the interface board mounted in each node device, and serves as a relation as shown on drawing 3. For example, as shown on drawing 3 in this example, when «the node device / line number A» is registered into the «priority 1» of the clock extraction circuit priority table 5, the «line number A» of the circuit connected to the interface board 1 mounted in the node device (A-D) 1 is shown, and this «line number A» serves

as a circuit which is extracting the present clock. And if line number B-N connected to interface board n from the remaining interface boards 1 is registered sequentially from the «priority 2» of a clock extraction circuit priority table, when a clock abnormality occurs, a clock is extracted from the circuit of the «line number B» connected to the interface board 1 which «the node device / line number B» of «the priority 2» show, and clock relief can be performed. Next, the case where a row order of the line number of «the priority 1» to the «priority n» of the clock extraction circuit priority table 5 when a clock abnormality occurs is updated is explained with reference to drawing 4. As shown on drawing 4, in this example, the line number of the line segment is registered into the clock extraction circuit priority table 5 times, and the state where «the line number E» was registered into «the priority 5» from «the line number A», respectively is shown on it from «the priority 1» at the time of first time line number registration.

[0026] And if a clock abnormality occurs while getting it blocked and extracting the clock from the «line number A» of «the priority 1», the state shown on drawing 4 (a) in this case, and, a clock extraction circuit priority table will change in the state of drawing 4 (b). Namely, the «line number A» information which shows the number of the circuit which was extracted in drawing 4 (b) until the clock abnormality occurred, it moves to the end of a table, and becomes «the priority 5», and the «line number B» information registered into «the priority 2» from the first is instead advanced to the «priority 1» with the highest priority of clock extraction. Thus, a clock is extracted

from the circuit of «the line number B», and clock extraction is relieved. As for other «line number C» - «line number E», in drawing 4 (b), beforehand is advanced to «priority 2» - «priority 4», respectively.
[0027] When a clock abnormality is detected from the state of drawing 4 (b) that is, in the case where a clock abnormality occurs twice from the state shown on drawing 4 (a), it changes in the state shown on drawing 4 (c). Namely, the «line number B» which shows the number of the circuit which was extracted in the state of drawing 4 (b) in drawing 4 (c) until the clock abnormality occurred. It moves to the end of a table, and becomes «the priority 5», and the «line number C» registered into «the priority 2» from the first is instead advanced to the «priority 1» with the highest priority of clock extraction. Thus, a clock is extracted from the circuit of «the line number C», and clock extraction is relieved. As for other «line number D» - «line number A», in drawing 4 (c), beforehand is advanced to «priority 2» - «priority 4», respectively.
[0028] Next, about processing operation after a clock abnormality actually occurs until it changes the clock extraction point, drawing 5 is made reference and explained. Drawing 5 is a drawing showing the composition of the node monitoring instrument 3 shown on drawing 1. In drawing 5, the clock abnormality can detect a clock abnormality by polling the PLL status of the hardware which is carrying out clock extraction. If a clock abnormality is detected in the midst of carrying out clock extraction with the line number A of the priority 1 registered into the clock extraction circuit priority table 5,

a clock abnormality will be notified to the problem management section 6, and directions of a change demand of the clock extraction point will be taken out from the problem management section 6 to the clock control section 7. In the clock control section 7 with which directions of the clock extraction point change were taken out, a clock is changed from the line number A registered into the priority 1 to the line number B of the following priority. In that case, it is original with the clock control section 7 in the clock abnormality not having occurred in the changed line number, and PLL status is checked, and if unusual, it changes to the following priority further.

[0029] Although this example explained that the node monitoring instrument 3 had the mentioned above function, it shall not be limited to this and each node device (A-D) 1 shall possess.

[0030] If the maintenance person is registering the line table last time clock extraction in advance as clock relief in the case of extracting the clock source from external devices (SDH end and the like) with ring network composition according to the composition explained above, as the clock extraction point changes automatically, power is dramatically demonstrated to the clock relief on a ring network.

[0031] Although invented by development by a ring network this time, as an applicable field, it shall be applicable also to the system of the star formed network which uses ATM.

[0032] Next, the 2nd invention is explained.

[0033] Drawing 6 is a drawing showing the composition of the communication system according to the 2nd

invention. As shown on drawing 6, in this communication system to the clock board 10. The selector 110 which chooses any one from a network clock, an external clock or a running clock in this selector 110, and a clock stop is detected for every clock, the clock rate malfunction detection section 112 which detects the abnormalities in speed of a clock for every clock with the clock stop primary detecting element 111 which notifies to the control section 11 by making this detection result into alarm information, and is notified to the control section 11 by making this detection result into alarm information, it is in the latter section of the mentioned above selector 110, and PLL circuit 113 and the frequency divider 114 which carry out dividing to a frequency clock component required of other substrates based on the clock in which the selected output was carried out by the selector 110 are provided, and it is constituted. It is distributed as various clocks generated as mentioned above in PLL circuit 113 and the frequency divider 114, and also the clock by which the selected output was carried out by the selector 110 may be distributed as 8 kHz as it is.

[0034] Detection of the clock stop according to the surveillance of a clock rate, namely, the clock delay of fixed time, in the preceding paragraph of the selector circuit 110 which chooses a master clock according to this composition, the clock of a cycle quicker than the clock of 8 kHz of basic clocks is detected, the selected output clock of selector 110 based on the alarm information which raised these each detection result to the control section 11 as alarm information, and has gone up by this control section 11 that it was made to carry out switching

control, while being able to prevent preliminary the adverse effect of the clock done to other substrates by the quick clock which was not relieved conventionally being undetectable, as it can control, so that a clock chooses a normal certainly when performing a clock change, the normality of the clock after the clock change which is not in the former can be guaranteed.

[0035] Next, the circuitry of the clock stage primary detecting element 111 and the speed malfunction detection section 112 shown on drawing 6 are explained.

[0036] Drawing 7 is a drawing showing the time chart which shows the relation between the signal inputted and the signal outputted to the circuitry and these each circuit section of the clock stage primary detecting element 111 and the speed malfunction detection section 112 shown on drawing 6, drawing 8 (a) shows the circuitry of the clock stage primary detecting element 111 and the speed malfunction detection section 112, and both have adopted 123 (Dual Retriggerable Monostable Multibrators With Clear) IC as a detector circuit in this example. The 8 kHz clock which drawing 7 (b) shows the time chart of the input signal in these each circuit, and an output signal and into which the above drawing is inputted in the clock stop primary detecting element 111, it is a time chart which shows the relation of the clock stop alarm signal outputted from the clock stop primary detecting element 111, and the following drawing is a time chart which indicates the relation of the speed abnormal signal outputted from the speed malfunction detection section 112 to be the 8 kHz clock inputted into the speed malfunction detection section 112.

[0037] And although it aims at supervising from which a clock turns into a master clock whether it is uniformly inputted at 8 kHz in these clock stage primary detecting element 111 and the speed malfunction detection section 112, as these decision contents, the clock stop primary detecting element 111 makes a «clock stop» the case where a clock is inputted a cycle later than 8 kHz, as usual, and the clock rate malfunction detection section 112 makes conversely the case where a clock is quicker than 8 kHz «the abnormalities in speed».
[0038] And the clock stop primary detecting element 111 uses the standup waveform of a clock as edge like the conventional method, and with external resistance and capacitor capacitance value. When there is no fixed time A (example: A > 125 μs + 10%) unusual edge detection, a clock stop is detected because Q bar output serves as «H» (when it is got blocked and there is no clocked into).
[0039] On the other hand, although the clock rate malfunction detection section 112 uses the standup waveform of a clock as edge like a clock stop as a method, by making external resistance and capacitor capacitance value into a value which brings forward the detection time B (example: B < 125 μs - 10%). If the clock is normal, the edge of an input signal will not be detected, but an output signal will serve as «H» judge that is a clock quicker than a detection condition if it becomes «L» and edge is detected.
[0040] According to this composition, the clock of a cycle quicker than the 8 kHz clock used as a master clock can be detected, and, thus, a possibility of inducing

malfunction in PLL circuit 113 can be prevented preliminary.
[0041] Next, the 3rd invention is explained.
[0042] Drawing 8 is a drawing showing the composition of the communication system according to the 3rd invention, and in this communication system, the clock board 12 which carries out dividing used to generate system clock, the interface board 13 connected with an external net or a terminal, and the switch board 14 which performs switching processing of the data from this interface board 13, the control section 15 which controls these substrates during communication, it is carried out in the form in sync with the clock of versatility distributed from the clock board 12.
[0043] Next, when the clock which it is mounted in the interface board 13 and received through the switch board 14 from the clock board 12 is normal, LSI (a cell transmission section) which transmits an invalid cell even if the effective cell is not inputted, perceive a cell receive section, and loopback setting out is carried out, so that the cell from the cell transmission section 131 can be received in the cell receive section 132, the mechanism in which it can know that the clock generated with the clock board 12 is normal at an early stage by checking that the empty cell is flowing at the time of power supply starting is realized.
[0044] According to this composition, with the clock board 12 shown on the mentioned above example, the clock which was generated is extracted, at the time of the standup of a device, normality can be quickly checked.

[0045]
[Effect of the invention] According to the 1st invention as explained above, the memory means which stores the priority information which shows the priority of clock extraction corresponding to the circuit information connected to the source of an external clock, the clock extraction point switching control means which performs switching control of the clock extraction point based on the information stored by the memory means, when a clock abnormality was detected, if the maintenance person is registering line information before clock extraction in advance, while being able to change the clock extraction point automatically and being able to perform clock relief at an early stage by that cause, a maintenance person's time and effort can be saved.
[0046] According to the 2nd invention, a clock detection means performs detection of a clock stop, and detection of the abnormalities in a clock rate for every clock of a selection circuitry, the clock switching control means which controls the change of a clock which carries out a selected output in a selection circuitry according to the result of this detection, even when the abnormalities of the master clock by which the selected output was carried out working are discovered, by the clock detection means in the selector, it can change to the clock with which normality was guaranteed, and also becomes suppressing generating of abnormal operation, and communicative reliability can be improved.
[0047] According to the 3rd invention, the clock extracting means which extracts a clock from the source of an external clock, a data forwarding means to receive

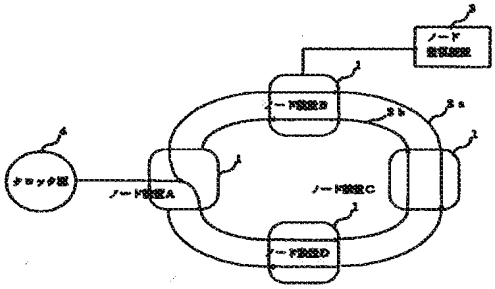
the normal clock outputted from a clock extracting means, and to perform sending operation of valid data or invalid data, the clock normality verifying means which checks the normality of the clock which judges whether data was sent out from the mentioned above data forwarding means at the time of a power supply standup, and is outputted from the mentioned above clock extracting means, the reliability of the master clock before operation and various clocks in which dividing is carried out and are distributed to each of other substrate can be raised, and the problem after power supply starting can be reduced.

[Brief description of the drawings]
[Drawing 1] is the drawing showing the example of 1 composition of the communication system according to the 1st invention.
[Drawing 2] is the drawing showing the composition of the clock extraction circuit priority table according to this invention.
[Drawing 3] is the drawing showing the relation between the clock extraction circuit priority table and the line number of a node device shown on drawing 2.
[Drawing 4] is the drawing showing an example in case a row order of the priority of the clock extraction circuit priority table 5 when a clock abnormality occurs is updated.
[Drawing 5] is a drawing showing the composition of the node monitoring instrument 3 shown on drawing 1.
[Drawing 6] is the drawing showing the entire configuration of the communication system according to the 2nd invention.

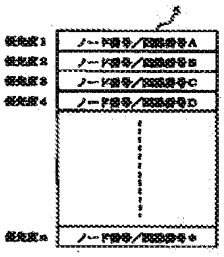
[Drawing 7] is the drawing showing the time chart which shows the relation between the signal inputted and the signal outputted to the circuitry and these each circuit section of the clock stage primary detecting element 111 and the speed malfunction detection section 112 shown drawing 6.
[Drawing 8] is the drawing showing the composition of the communication system according to the 3rd invention.
[Drawing 9] is the drawing showing the composition of the conventional communication system.
[Drawing 10] is the drawing showing the composition of the clock board in the communication system shown on drawing 9.

[Description of numerals]
1 Node device (A-D)
2a, 2b Duplex transmission line
3 Node monitoring instrument
4 Clock source
5 Clock extraction circuit priority table
6 Problem management section
7 Clock control section
10 Clock board 11 Control section
111 Clock stop primary detecting element
112 Speed malfunction detection section
113 PLL circuit
114 Frequency divider
12 Clock board 13 Interface board
131 Cell transmission section
132 Cell receive section
14 Switch board 15 Control section

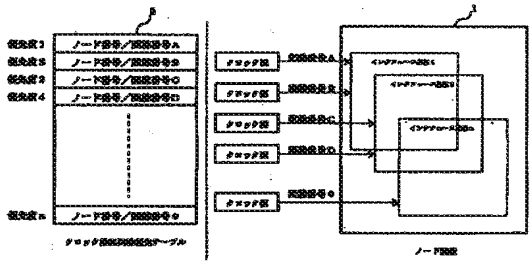
Drawing 1



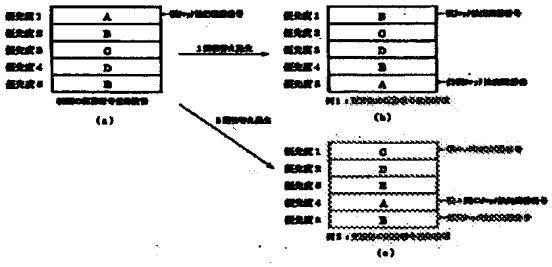
Drawing 2



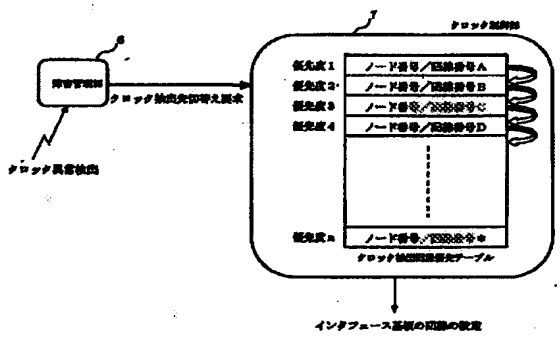
Drawing 3



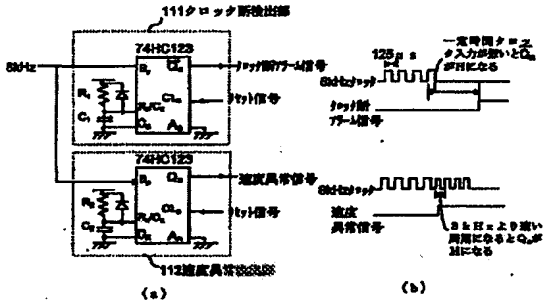
Drawing 4



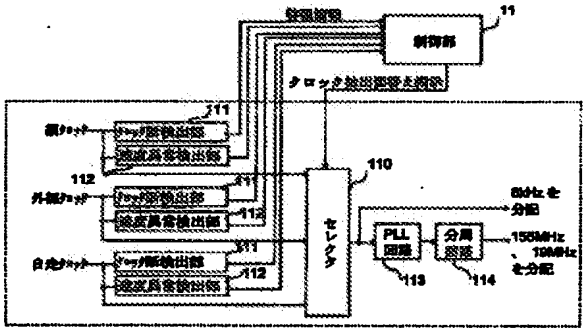
Drawing 5



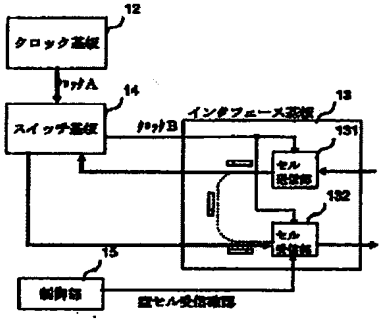
Drawing 7



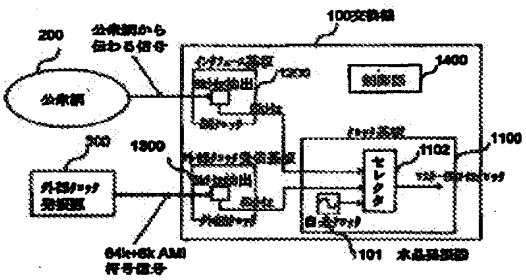
Drawing 6



Drawing 8



Drawing 9



Drawing 10